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Solid State Pre-Formed Electronics Adhesive (SPEA)

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Solid State Pre-Formed Electronics Adhesive (SPEA)

by

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Abstract

In mobile and handheld consumer electronic markets, product use conditions drive the requirement for mechanical strength and device durability. The majority of relatively large form factor electronic components in a laptop, mobile internet device, PDA, or mobile phone use an adhesive as a stiffener to help protect the component from physical stresses imposed by daily wear and tear. Described herein is an innovative solution referred to as Solid State Pre-Formed Electronics Adhesive (SPEA), which enables a decrease in circuit board manufacturing throughput time while increasing mechanical durability with a consistent and characterized adhesive application process.

Today, many consumer electronic ODM's (Original Design Manufacturers) and CM's (Contract Manufacturers) use a liquid adhesive dispensed after placement of an electronic component within the SMT (Surface Mount Technology) process. On average, this adds up to 60 seconds to the throughput time of a typical motherboard as the material needs to be applied and then cured. In addition, the current adhesive dispense application process is not tightly controlled and is highly variable depending on operator, material type, and circuit board density. Data will demonstrate that the effect of the adhesive deposition profile and consistency in application directly affects repeatable margin increase gains in a dynamic stress event.

In partnership with a specialty chemical company, a unique thermoset epoxy compound was designed to provide maximum component to circuit board interconnect strength while maintaining its form at ambient temperatures. When applied to electronics manufacturing, the compound referred to as research resin RSM-3696 has the following advantages over current solutions:

1. **Reduced Manufacturing Processing Time:** Enables a solution that can be transitioned transparently into a circuit board manufacturing facility which reduces the average processing time for a typical device motherboard.
2. **Improved Application Repeatability:** Enables a solution that increases adhesive deposition consistency and placement repeatability, critical in achieving improved dynamic performance.
3. **Delivers a Reference, Characterized Solution:** Current industry adhesive application techniques and materials vary widely and component manufacturers cannot validate reliability performance with a confident baseline. This is due to the high variability of performance in commercially available adhesives. SPEA provides a characterized adhesive solution with a clear baseline margin increase on which to evaluate dynamically stressed system performance.

The need to continually increase the resistance to component damage through dynamic testing is a critical aspect to consider given market trends and device roadmaps. Large component manufacturers have the opportunity to further embed themselves into untapped markets where portability and performance converge and drive the need for more robust packaging solutions. The development and application of SPEA will continue to maintain silicon and packaging reliability as consumer devices continue to shrink, becoming ever more portable.

Dedication

To my beloved parents, Thomas Charles Cope and Molly Alexander, for raising me with a sense of pride, thoroughness, accountability, and most importantly the self-realization of the importance of dedication, in all aspects of life. Also to Ruben Rodriguez-Torres and William Berry, for your guidance, coaching, and mentorship over the past 9 years. You were taken far too early, but you imprinted my life with your kindness and friendship. I miss you both dearly.

Table of Contents

List of Tables

List of Figures

1. Introduction

1.1 - Problem Statement:

Electronic packaging, typically consisting of a silicon die soldered to a printed circuit board (PCB) substrate, continues to decrease in physical size while interconnect input / output (IO) count and speed increase. When IO increases, the number of soldered connections at the second level interconnect (SLI) also increase leaving less physical real-estate for each soldered connection. As one might expect, this yields a reduction in solder joint size and in turn a decrease in interconnect surface area. Combined with consumer demand for increased device mobility, this trend has created a challenge for electrical-mechanical designers to meet both dynamic and static mechanical targets.

For many years Original Equipment Manufacturers (OEM) have employed industry best practices when designing end products for reliability, a common industry term for this is DfR or Design for Reliability (Engelmaier, 2008). Specific to mechanical DfR, when a device's use conditions require mobility, designers often use liquid adhesive during the board manufacturing process to compensate for intended use and progressive form factors, increasing dynamic performance.

The liquid adhesive acts to bond the substrate to the motherboard while not interfering with the electrical connectivity of the assembly. An example of substrate to motherboard adhesion via a corner bonding process can be seen in Figure 1; the component from the recently released Samsung Galaxy S3 is the Exynos CPU, a 1.4GHz quad-core ARM processor built on a 32nm process, photo compliments of iFixit and Chipworks (2012).

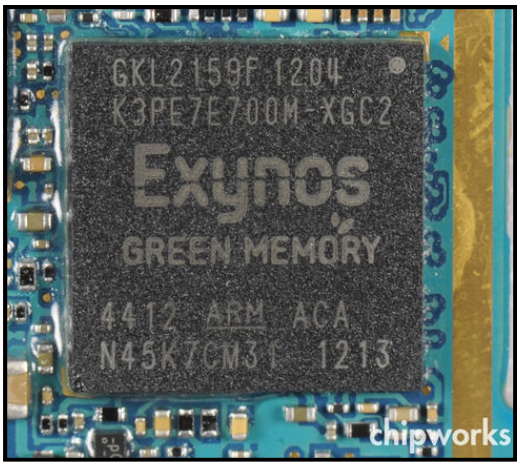

Figure 1 - Samsung CPU with Corner Bond Adhesive (iFixit & Chipworks, 2012)

Board-level adhesive technologies can be categorized into the following types: full fill and corner fill, both relying on capillary action and wicking for under fill, and corner glue, a direct bond of the substrate edge to the motherboard; a visual representation of these types can be found in Figure 2.

Many consumer-known adhesive brands, such as 3M and Loctite, have developed unique adhesive formulations for the electronics industry; however, all take the form of a liquid at room temperature, limiting the range of application techniques and processes. Research has proven that variability induced during the application process, being caused by many

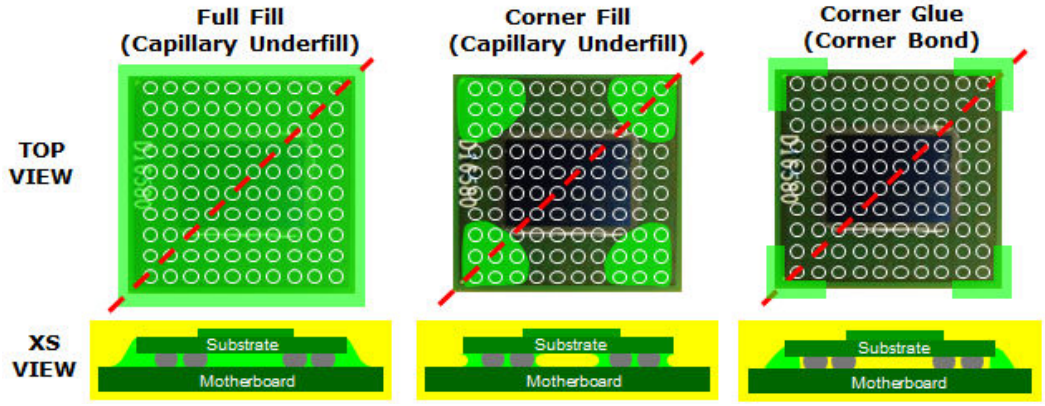

Figure 2 - Types of Board-Level Adhesive Technologies (Intel Corporation, 2006)

factors, significantly limits the effectiveness of the adhesive, in some cases providing no additional performance increase. The inability for electronic component manufacturers to assess performance of their component in varying designs due to variability in both the design and the manufacturing process is driving the evaluation of pre-applied adhesives.

1.2 - Current Industry Adhesive Application Processes:

Current manufacturing processes apply liquid adhesive using a variety of techniques. These can be categorized into manual, application by hand, or automated, using computer controlled equipment.

1.2.1 – Manual Adhesive Application:

Manual processing is predominant in high volume manufacturing (HVM) applications; this is largely due to the geography of manufacture and associated labor costs, where a large capital equipment purchase may not provide adequate return on investment during the build lifecycle of a single product. Manual application processes consist of an operator using either a manual or pneumatic syringe to dispense adhesive in a prescribed location. The deposition location is often controlled by operator work instructions or at times demarcated silkscreen printed onto the PCB. In either situation, the result of a manually deposited liquid adhesive is highly variable and largely based on the operators experience and technique, both of which are difficult to maintain and control.

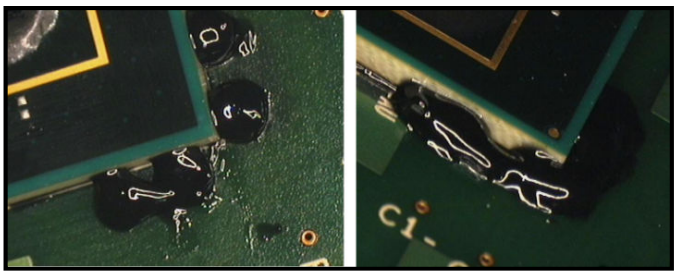

Figure 3 - Operator Induced Adhesive Deposition Inconsistencies

1.2.2 – Automated Adhesive Application:

In recent years, automated adhesive application has increased in popularity, in part due to reasons discussed. Large Surface Mount Technology (SMT) equipment manufacturers such as DEK, Fuji, and Panasonic have begun to invest in unique ways to integrate adhesive application into existing equipment. An interesting example of this is DEK's adhesives screen-print process which integrates acrylic stencils and custom settings into standard solder paste-print equipment (DEK, 2013). The highest occurrence of automated adhesive dispense, however, comes by way of pneumatic heads integrated into SMT placement equipment. Additional 'flexible' heads can be purchased and fit into placement machines leveraging on board mechanical systems that are needed for component placement. Figure 4, compliments of Panasonic Panasert (2002) depicts a screw release adhesive dispense head fit to a common Panasonic SMT placement platform.

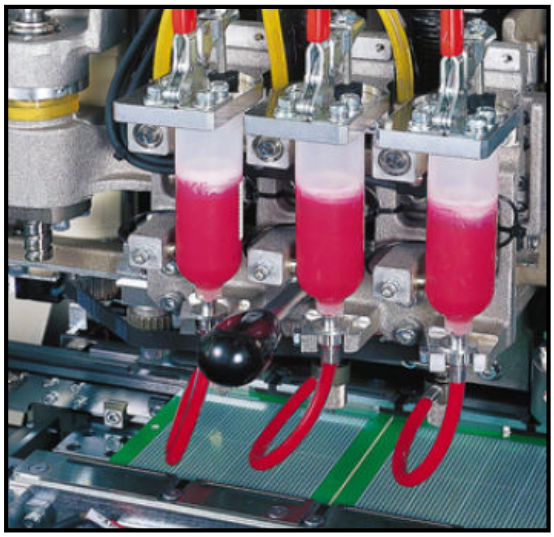

Figure 4 - Flexible Automated Adhesive Dispense Head (Panasonic, 2002)

Advantages in integrating this capability are similar with all other automated processes: higher board throughput, increased deposition consistency, and a decrease

in material waste. This comes at the cost of a reduction in component placements, however, as a single head within the machine is consumed as an adhesive dispenser. Further, typically only a small subset of total components will be glued to the motherboard leaving the adhesive dispense head largely idle during board processing.

1.3 – Scope and Limitations of Research:

Experimentation and results will focus on evaluation in two principal categories, manufacturability and dynamic-shock reliability. Requirements and specifications supporting evaluation categories are outlined in section 2.1 and discussed in section 2.2. A single preformed material developed in partnership with a specialty chemicals company and referred to as Epoxy Research Resin RSM-3696, Cariverse 200, or SPEA, will be evaluated against a control group using no adhesive. Manufacturability results will largely be binary confirming that current industry acceptable processes and parameters can be used to effectively work with the equipment. Additional specific success criteria and metrics will be detailed to support both categories throughout the discussion, however, when not explicitly stated, current industry baselines will be used to assess the significance and viability of results.

Both high volume electronics manufacturing and subsequent reliability evaluations are a capital intensive process, primarily due to material and equipment cost. Thus, throughout this discussion, unique methodologies will be employed to perform comparative assessments limiting unnecessary investment in materials and evaluation expense.

1.4 – History of Epoxy Research Resin RSM-3696:

Research Resin RSM-3696, later branded as Cariverse 200, and referred in this application as SPEA, was co-developed by a large electronic component manufacturer and a specialty chemicals company in 2005. The purpose of the thermally reversible network polymer resin was to be pre-applied to an electronic component substrate after component assembly and prior to board assembly. The polymer blend was formulated such that its thermal characteristics parallel a typical lead-free reflow profile causing no disruption to typical lead free solder reflow processing requirements, reference Figure 5 for a summary of physical material characteristics throughout a temperature cycle event (Intel Corporation, 2007).

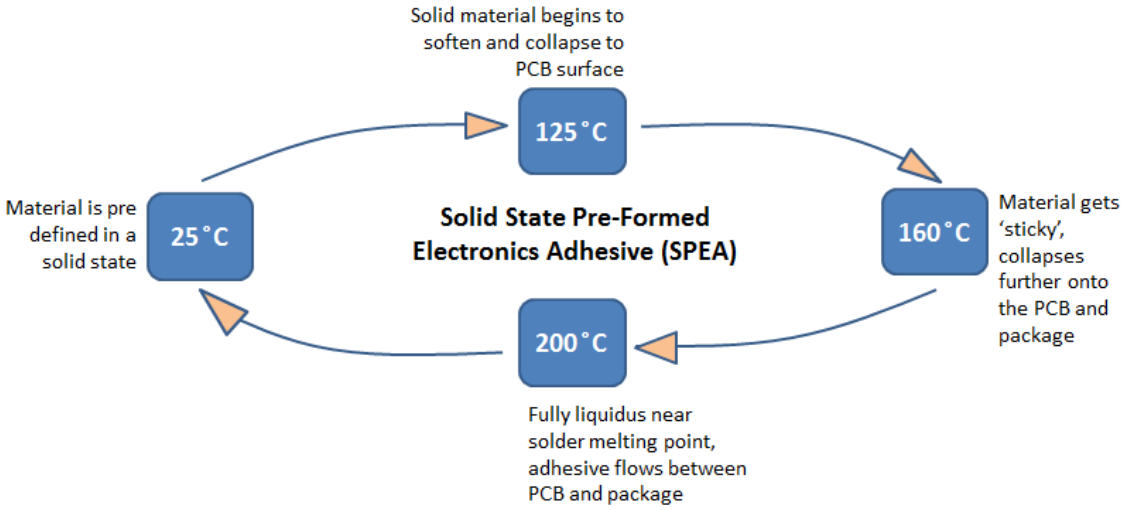

Figure 5 - Summary of SPEA Phase Changes throughout Temperature Cycle (Intel Corporation, 2007)

Formulations prior to 2005, branded as Cariverse 100, were evaluated for similar applications. Summaries and the results of relevant studies can be found in United States patents, in IEEE (Institute of Electrical and Electronics Engineers) publications, and are referenced throughout this discourse (Dunlap, 2005). Cariverse 200 was modified slightly in 2005 to adjust for reliability risks, predominately with thermal cycling stresses and

associated mismatches in bonded materials coefficient of thermal expansion. Evaluation and results discussed herein have been made against Cariverse 200.

1.4.1 – Epoxy Research Resin RSM-3696 (Cariverse 200) Material Properties:

The following table lists measured, typical material properties for Cariverse 200. Measurements were made and data collected in partnership with the specialty chemicals company prior to manufacturing and reliability evaluations.

Table 1 - Material Properties for Cariverse 200 Epoxy (Intel Corporation, 2007)

Material Property	Nominal Value
Dielectric Strength	$375\,\frac{V}{10^{-3}in.}$
Dielectric Constant (ε_r)	$3.7\ at\ 1.0\ MHz$
Dissipation Factor (DF)	0.02%
Coefficient of Thermal Expansion (α_v)	$75\ \frac{ppm}{℃}$
Flexural Modulus (E_x)	$550\ ksi$
Flexural Strength	$12\ ksi$
Water Absorption (60℃)	1.5%
Melt Viscosity (P)	$Variable: 5-15\ Poise$

1.4.2 – Thermomechanical Analysis of Cariverse 200:

Thermomechanical analysis (TMA) provides a measurement of change in dimension or a mechanical property while a sample of material is subjected to a temperature change. TMA results for Cariverse 200 are shown in Figure 6 relative to a typical anhydride epoxy; note the extreme difference in dimensional change throughout the temperature

gradient. Important observations to draw from these results as they pertain to an SMT specific application are as follows:

1. Cariverse has minimal expansion or deformation between ambient and 110 degrees Celsius which is a critical phase in a lead-free reflow profile. During these temperatures, solder is softening and flux within the solder is starting to burn away. Dimensional expansion in an adhesive during this time could be detrimental to the X and Y orientation of the package on the PCB land pads.

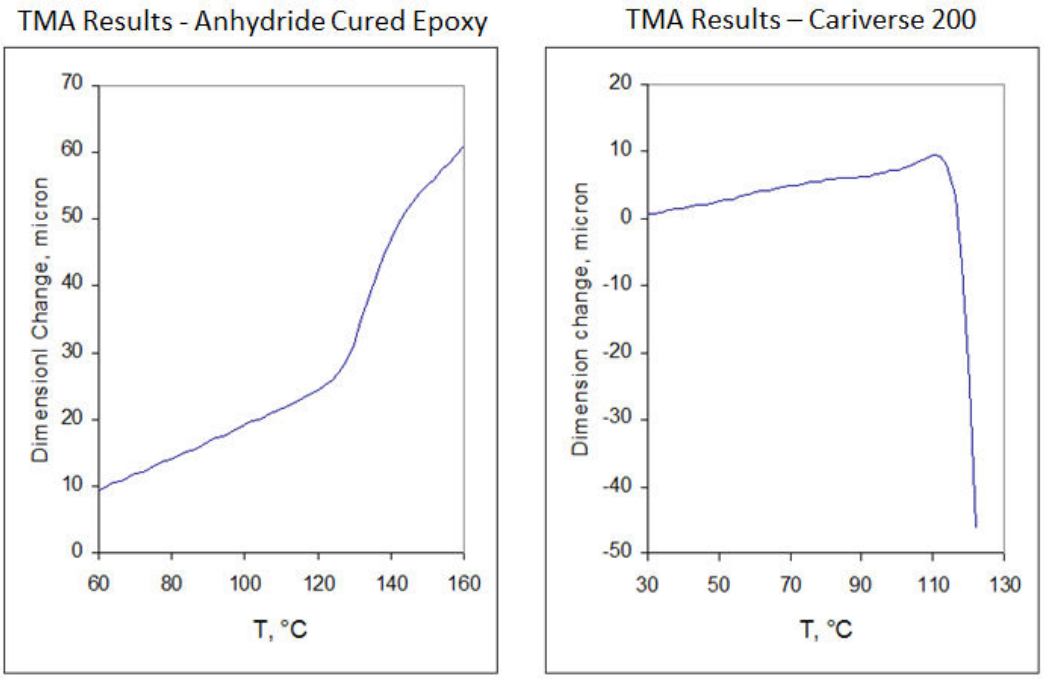

Figure 6 - TMA Comparison between Cariverse 200 and Anhydride Cured Epoxy (Intel Corporation, 2007)

2. At approximately 120 degrees Celsius there is a rapid retraction and collapse of the Cariverse adhesive material. This mechanism facilitates capillary flow under component edges and has proven to not negatively affect other solder joint quality indicators such as solder ball collapse, package standoff height, and

overall joint formation and shape, see section 4.4 for detailed analysis and results. Figure 7, below, is a potted cross sectional image of a component manufactured with SPEA. Note that the adhesive has flowed under the substrate to a depth of 2 solder balls.

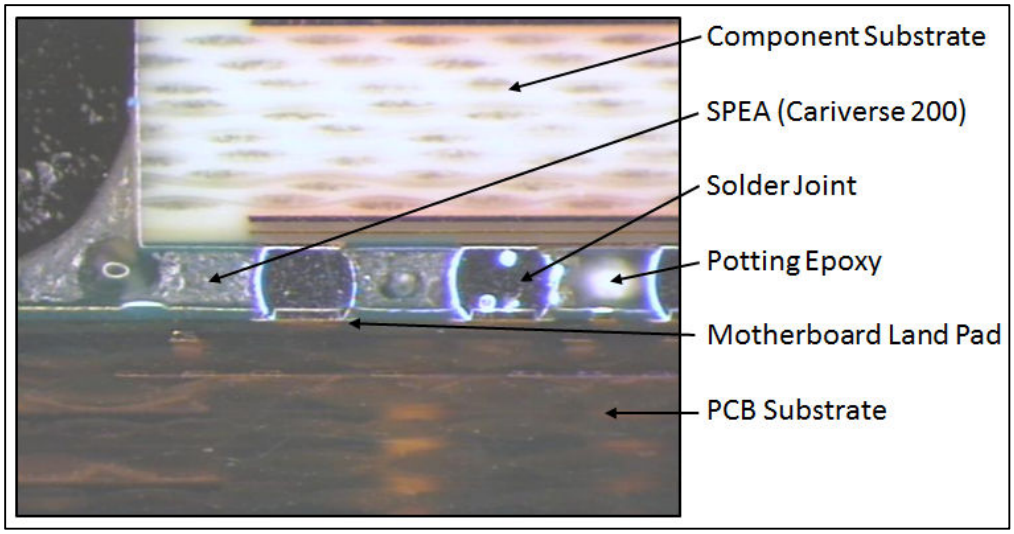

Figure 7 – SPEA Assembly, View in Cross Section (Intel Corporation, 2007)

1.4.3 – Polymerization Reactions:

Although not directly within the scope of assessment, it is important to reference material properties and related reactions creating thermo mechanical properties ideal for electronics manufacturing. In an IEEE publication made by B. Chang and others at the Westhollow Technol Center (1999), titled '*CARIVERSE*^{TM} *resin: a thermally reversible network polymer for electronic applications*', details of critical material reactions is paraphrased:

"These polymers [2,5-disubstituted furan resins and 2,4-bismaleimidotoluene] contain thermally reversible covalent crosslinks derived from the Diels-Alder addition of maleimide to furan. At elevated temperature, the crosslinks dissociate via a retro-Diels-Alder reaction to yield a low viscosity melt that readily polymerizes upon cooling to regenerate the network polymer" (p.49).

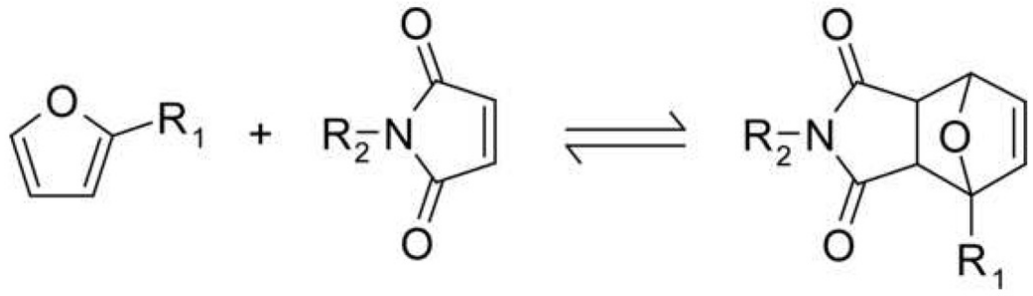

Figure 8 - Molecular Changes through Thermal Cycle (Adzima, 2008)

Figure 8 represents structural changes during heating and cooling cycles; the authors explain the reaction mechanism:

"Diels-Alder / retro-Diels-Alder reaction between a furan and maleimide. Polymer networks are formed when the Diels-Alder pathway is utilized in monomers with multiple reactive functionalities" (p.49).

2. Methods

2.1 – Requirements and Specifications:

The following table lists requirements and critical parameters evaluated within the scope of work, assessing manufacturability and dynamic reliability. Results, which will be discussed, will be presented relative to the requirement number, denoted in the first column of Table 2.

Table 2 - Study Evaluation Requirements and Specifications

#	Evaluation Category	Requirement Description	Metric (Value and Tolerance if Applicable)
1	SMT Manufacturing	Pick and Place equipment must be able to place preformed adhesive.	1. Yes / No
2	SMT Manufacturing	Reflow process must fit within typical lead free reflow profile – Reference Appendix A for target parameters.	1. T_{MAX} = 240-250°C 2. Time above Liquidus (TAL) = 60-90 seconds 3. Soak Time = 60-90 seconds 4. ΔT Across Component < 10°C
3	SMT Manufacturing	Manufacturing and post manufacturing, SMT assembly success indicators must be met.	1. No Solder Bridging 2. < 25% Joint Voiding 3. Statistically Equivalent Package Standoff Height 4. Qualitative Solder Joint Formation

#	Evaluation Category	Requirement Description	Metric (Value and Tolerance if Applicable)
4	BGA Rework	Rework process must fit within typical lead free rework profile.	1. T_{MAX} = 240-250°C 2. Time above Liquidus (TAL) = 60-90 seconds 3. Soak Time = 60-90 seconds 4. ΔT Across Component < 10°C
5	BGA Rework	Adhesive fully removed from PCB and surface clean, soldermask not compromised.	1. Yes / No
6	Dynamic Reliability	Equivalent electrical continuity with non-adhesive sample up to capability cliff.	1. $\Omega_{CONTROL} = \Omega_{SPEA}$ at Capability Cliff
7	Dynamic Reliability	Increased shock resistance in drop use condition.	1. Increase in ε_{MAX} without electrical degradation (increase in Ω)

2.2 – Evaluation Methodologies:

The following methodologies, and best known methods, were employed throughout data collection activities, yielding results presented in section 4, Results and Discussion. They are explained to provide the reader with an understanding and baseline for which results, conclusions, and recommendations are being made. Methodologies listed below are explained in ascending order according to requirements listed in Table 2.

2.2.1 – Thermal Profile Generation and Analysis (SMT & Rework):

Controlling the change in temperature (ΔT) across a motherboard during a reflow cycle is critical to ensuring minimal deviation in solder joint temperatures across multiple components. This in turn ensures a more uniformed joint collapse and coalescence. Building upon the genesis of this work, consumers demand for high functioning electronics in small form factors, manufacturers often find that X-Y spatial keep-outs are encroached by design teams working to fit within a finished design. Components act as thermal mass during reflow and detailed analysis and oven-tuning is required for each unique design.

Thermocouples are placed at strategic locations across an assembled motherboard. Thermocouple location is critical and is often informed by experienced reflow oven operators or process development engineers. Using an oven profiler, which measures and records multiple channels of temperature data throughout a reflow event, an operator works to reduce ΔT while maintaining critical solder paste and solder ball composition profile parameters. This is accomplished by varying oven temperatures in zones, which represent unique sections along the length of the oven, and top / bottom heaters; see Appendix A for common lead free reflow parameters.

An example reflow profile collected on a 14 zone Furukawa Electric Salamander (XNK-1245PC) is shown in Figure 9. This example was taken from a large server motherboard and therefore represents data from 17 unique thermocouples. Note that this amount of thermocouples on a profile-board is uncommon and most profiler equipment supports a maximum of 12 data channels.

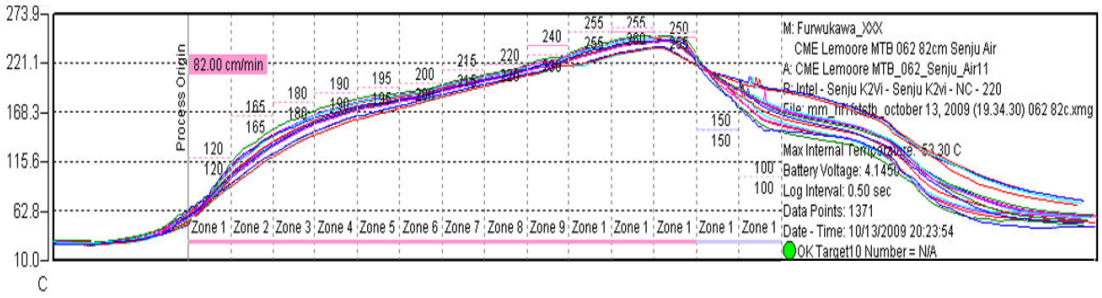

Figure 9 – Lead Free Thermal Profile Thermocouple Trace
(Note that this image can also be found in a more easily viewable format in Appendix C)

Note critical parameters which we can derive from the graph: Belt speed at 82 cm / minute (top left); Zone temperatures (top / bottom) recorded along the thermal profile trace; Number of oven zones, 12 heating and 2 cooling, noted along the X-axis.

Although some oven profile equipment manufacturers are beginning to offer automated profile quality assessments and predictive adjustments, analysis is most commonly done by skilled operators or engineers by hand. Critical parameters mapped against temperatures and times are analyzed and demonstrated in Figure 10.

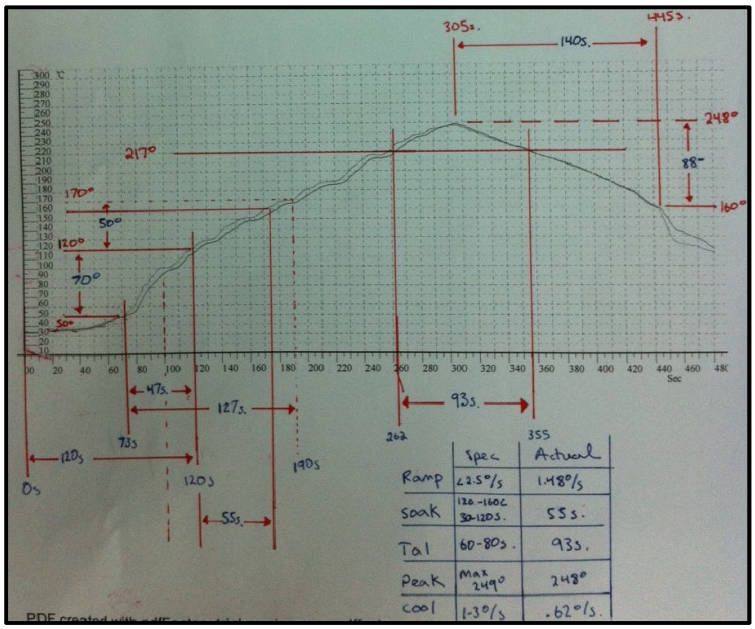

Figure 10 - Common Thermal Profile Assessment Technique
(Note that this image can also be found in a more easily viewable format in Appendix D)

2.2.2 – Electrical Resistance and Daisy Chained Connections:

Developing and manufacturing assembly test vehicles (ATV), replicating a functional finished component is an invaluable tool when qualifying the component for both manufacturability and reliability. It is critical that physical characteristics of the ATV match the functional component as closely as possible. Properties like total package thickness, die size (X-Y-Z), substrate thickness and layer count, laminate / resin type, solder resist opening (SRO) size, and others are all critically important to the validity of data generated from ATV evaluations.

During the design of an ATV, it is common practice to create daisy chained connections, such that when the ATV is mated with a corresponding PCB, chains of connections are formed and can be tested electrically by measuring continuity. Test points can be broken-out from any point in the chain and are often designed based on the suite of tests to be performed. For example, mechanical strains due to dynamic stresses on a square or rectangular package are highest at the extreme corners of the package. An industry standard test for determining transient strain capability, the three point bend test, is shown in Figure 11. The corresponding strain plot helps to visually

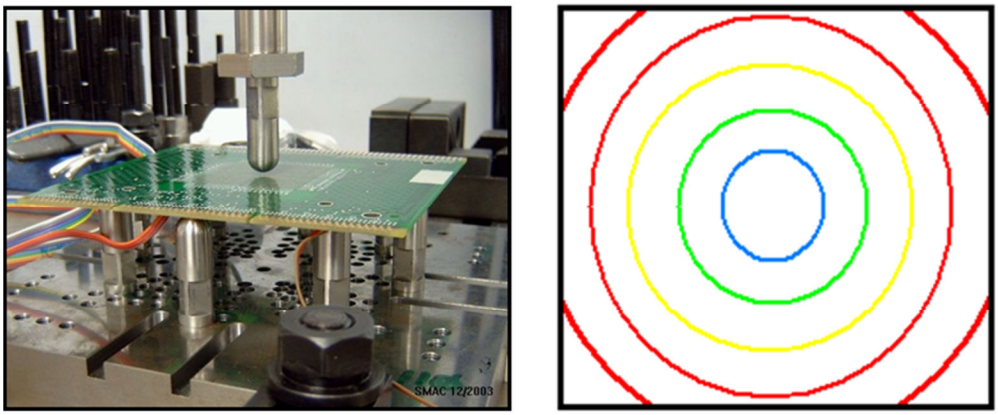

Figure 11 - Bend Test and Corresponding Strain Plot (Intel Corporation, 2008)

convey stress prorogation throughout the component during the test. Note that the primary bending mode that is of concern is one that puts the solder joints in tension versus compression.

In the example discussed previously, the primary concern or initial evaluation would be assessed against solder joints at the corner of the package. Thus, daisy chains allowing isolation of corner joints are ideal in assessing mechanical damage. A visual representation of a daisy chain connection between an ATV and a PCB is shown below.

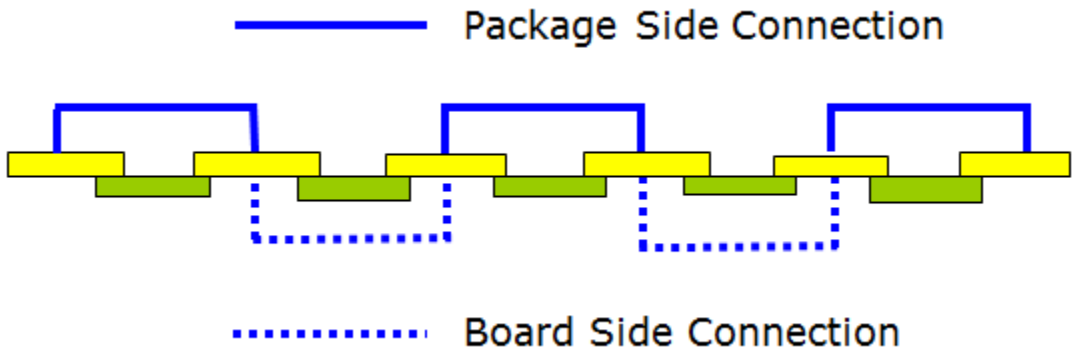

Figure 12 - ATV Package and PCB Daisy-Chain Representation

2.2.3 – Strain as an Indicator to Solder Joint Failure:

Strain as an indicator to solder joint failure is derived from the application of rectangular three-rosette strain gages, shown in Figure 13 (Vishay, 2010), and placed at the corners of a package, either on the package itself or on the PCB.

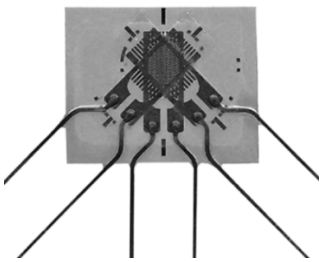

Figure 13 - Three-Rosette Strain Gage, Compliments of Vishay Precision Group (2010)

Detailed correlations are then run between input strains and solder joint crack percentages, allowing reliability engineers to assess component dynamic reliability performance in varying designs with a common baseline.

Diagonal strain (ε_d) defined by the equation below, has been found to most closely correlate with actual solder joint damage. Throughout this discussion, when a single strain value is presented, it is presented as a diagonal strain (Intel Corporation, 2008).

$$\varepsilon_d = Max\left[\varepsilon_2, \varepsilon_1 + \varepsilon_3 - \varepsilon_2\right]$$

Note that Figure 14 defines gage orientation as inputs into the calculation for the diagonal strain, also known as maximum allowable strain, (ε_d).

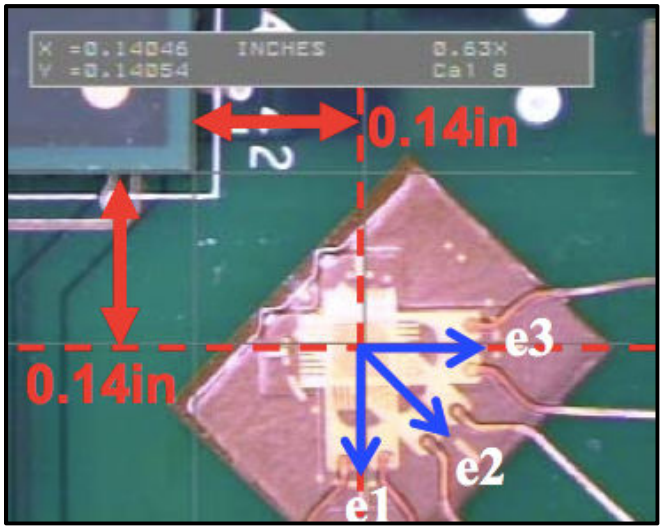

Figure 14 - Gage Location and Strain Vector Definition (Intel Corporation, 2008)

Given the definition of strain as the change in length divided by the original length (ΔL/L), it is easy to understand the importance of gage location relative to the package corner. Prior to strain joint damage correlation, gage location is defined as a critical

specification for all future assessments. General theory of strain gages as well as the specific electronics application being assessed is discussed in detail in section 2.3.

2.2.4 – Cross Sectional Analysis:

A more simplistic yet equally important methodology employed is the process of potting samples in a translucent epoxy for sectioning and analysis. Referred to as cross-sectioning, the process entails submerging a sample in liquid epoxy, removing all air from the mixture via vacuum, curing the epoxy, cutting the sample at the area of interest, and then polishing the cut edge for microscopic inspection. This process provides an ideal opportunity to measure static, post assembly manufacturing quality indicators, specifically discussed in requirement #3 of Table 2. For reference, Figure 7 is a cross-sectional image taken of an assembled SPEA package.

2.3 – Strain Gage Construction and Operating Principles:

Strain gages are used widely for varying mechanical assessments in many industries, from construction to aerospace to biomedical applications, the ability to monitor physical deflection as a function of resistance change is an invaluable mechanical tool.

While strain gage construction can widely vary, a modern day gage is typically constructed of a metallic foil applied to an adhesive backing in a serpentine pattern. When applied to a specific application, resistance is monitored at the ends of the foil chain and measurements taken throughout the activity or action being tested. Depending on many variables including, but not limited to, gage sensitivity, gage factor, physical foil geometry, and temperature, even the minutest deflection can be captured and measured by a strain gage.

Modern day strain gages as previously discussed also come in varying types and designs. Variations are largely driven by application and specific stress-strain states under test, but commonly vary the number of gages, the gage orientation relative to the unit under test, and the foil orientation relative to the unit under test. All of these variables must be designed and controlled closely depending on the application of the gage.

During research outlined in this text a Vishay WA-XX-060WR Series Tri-Rosette strain gage was used to monitor strain during simulated drop events. The specific Tri-Rosette gage used is designed and constructed by stacking three gages atop each other and orienting the unique gages at 0, 45, and 90 degrees; reference figures 13 and 14 for visual representation of gage orientation. While not all stacked gages span 90 degrees (some span 120 and even 180 degrees), this orientation is the most suitable based on the application being tested, this assumption will be further discussed in subsequent text. To reiterate, selection of a strain gage based on the testing application is absolutely critical. Orienting the long axis of the gage in parallel with the critical stress-strain vector allows for the gage to undergo maximum resistance change within the specific axis. The gage is most sensitive when the long axis of the foil serpentine is parallel with the stress-strain vector being tested.

During testing outlined in text, because of the shape of the assembly and package being tested, a 90 degree gage is most applicable. Gage location correlates to an arbitrary coordinate system defined by the edges of the package being tested, X and Y. The gage monitors vectors e1, e2, and e3 which correlate to package edges (X and Y) and the center of the package array (45 degrees). Again, see figure 14 for gage vector definition.

Monitoring three independent two-dimensional strain states, however, may not adequately represent the highest and most important strain values, shear strain and principle strain. Employing the formula in section 2.2.3, diagonal strain or principle strain can be computed and through multiple experiments has been found to most closely correlate to solder joint fatigue.

The methodology used and discussed herein is further supported and referenced by industry consortia, IPC and JEDEC. Specifically, standard 9704 provides detail to the methodology including materials, specifications, tools, and measurement (Jumho, 2013).

2.4 – Dynamic Reliability:

Dynamic reliability is defined as an assembly's resistance to electrical failure throughout a simulated drop event, where an assembly is defined as an electronic package soldered to a PCB. During evaluations intended to meet requirements #6 and #7, as outlined in Table 2, a simulated drop event is the input parameter. Measured outputs, thoroughly detailed in sections 2.2.2 and 2.2.3, are electrical connectivity (Ω) and strain (ε). While we are concerned with the magnitude, direction, and duration (pulse or period) of the input, it is most important to ensure its consistency throughout testing. When we eliminate the input as a variable, we are able to focus on our chief concern, which is of the measured outputs as an indicator to dynamic reliability.

Under this evaluation, a half-sine dynamic shock profile is employed. The acceleration (magnitude), as measured in G's, where G equals 9.8 m/s^2, is varied throughout testing to achieve higher peak strain values in turn resulting in higher resistance values (until a catastrophic failure is encountered in which resistance is undefined as the circuit is open).

2.5 – Tools, Capital Equipment, and Consumable Materials:

The following table lists tools, equipment, and consumable materials used throughout data collection activities. Items are listed by requirement number from Table 2, column A.

Table 3 - Tools, Capital Equipment, and Materials used During Evaluation

#	Type	Functional Description	Manufacturer / Model
1	Capital Equip.	Pick and Place Equip.	Universal Genesis GSM1
	Material	Solder Paste	Senju M705-GRN360-K2-Vi (SAC305, LF)
	Material	Adhesive Preform	Cariverse 200
2	Capital Equip.	Reflow Oven	Furukawa Electric Salamander (XNK-1245PC)
	Tool	Reflow Oven Profiler	SlimKIC 2000
	Tool	Thermocouple	Standard, K-Type Thermocouple
	Material	Oven Environment	N^2, O^2 < 3000 PPM
3	Capital Equip.	Solder Paste Printer	DEK Infinity 01
	Capital Equip.	Automated X-Ray Inspection	Agilent Medalist 5DX
	Tool	Multimeter	Fluke Digital Multimeter 115
	Tool	Paste Deposition Stencil (PCB)	Custom, Laser Cut, .005” mil Thickness, 1:1 Aspect Ratio
4	Capital Equip.	BGA Rework Equipment	SRT 1100 HR
	Tool	Paste Deposition Stencil (BGA)	Custom, Laser Cut, .005” mil Thickness, 1:1 Aspect Ratio
	Material	Liquid Flux	Kester 186 – Rosin Flux Pen
	Material	Solder Paste	Senju M705-GRN360-K2-Vi (SAC305, LF)
6, 7	Capital Equip.	Shock Table	Lansmont 1800-5
	Tool	Strain Data Logger	Kyowa PCD-300A
	Tool	Multimeter	Fluke Digital Multimeter 115
	Material	Strain Gage	Vishay WA-XX Tri-Rosette

3. Experimental Design

3.1 – Design of Experiment:

Experimental design, bound by limitations and scope outlined in section 1.3, is focused in two principle categories: manufacturability and dynamic reliability. The primary variable modulated under this evaluation was the application of SPEA versus a non-adhesive control group. A total of 36 assemblies were manufactured, 18 with SPEA and 18 without; each sample was assigned a unique serial number as outlined in Table 4. 'S' denotes an SPEA sample while 'C' denotes a control sample.

Details of the methods under which each sample was tested, are outlined in section 2, Table 2. The evaluation category column in table 2 corresponds with the evaluation category column below, in Table 4.

Table 4 - Sample Serialization Map

Serial Number	Evaluation Category
S1	Dynamic Reliability
S2	Dynamic Reliability
S3	Dynamic Reliability
S4	SMT Quality
S5	SMT Quality
S6	SMT Quality
S7	SMT Quality
S8	SMT Quality
S9	SMT Quality
S10	SMT Quality
S11	SMT Quality
S12	SMT Quality
S13	SMT Quality
S14	SMT Quality
S15	SMT Quality
S16	Rework
S17	Rework
S18	Extra

Serial Number	Evaluation Category
C1	Dynamic Reliability
C2	Dynamic Reliability
C3	Dynamic Reliability
C4	Thermal Profile
C5	Extra
C6	Extra
C7	SMT Quality
C8	SMT Quality
C9	SMT Quality
C10	SMT Quality
C11	SMT Quality
C12	SMT Quality
C13	SMT Quality
C14	SMT Quality
C15	SMT Quality
C16	SMT Quality
C17	SMT Quality
C18	SMT Quality

3.2 – Component / PCB Design Attributes:

The following sub sections outline critical physical characteristics of raw materials used during testing, specifically the PCB and the component test vehicle.

3.2.1 – BGA Test Vehicle Package Attributes:

The BGA test vehicle used for evaluation is of typical physical characteristics to a small form factor CPU or chipset often designed into tablet computers and smartphones. The test vehicle is both a Daisy Chain Test Vehicle (DCTV), with internal routing to support electrical continuity testing as outlined in section 2.2.2, and a Thermal Test Vehicle (TTV) with heaters in the die able to simulate operational temperatures. Note that under this evaluation TTV capabilities were not used. The following table, from Intel Corporation (2008), outlines critical physical attributes of the package evaluated.

Table 5 - BGA Test Vehicle Package Attributes (Intel Corporation, 2008)

Package Attribute	Value (Nominal)
X,Y Dimensions (Substrate)	22 X 22 mm
Substrate Thickness	0.662 mm
Solder Ball Count	956
Minimum Ball Pitch	0.6732 mm
Solder Ball Diameter	0.762 mm
Non Critical to Function Solder Balls	26
Solder Ball Pattern	Grid Array on 45 Degrees
PCB Pad Configuration	Combination MD & SMD
Package Pad Definition	SMD, 0.3 mm SRO

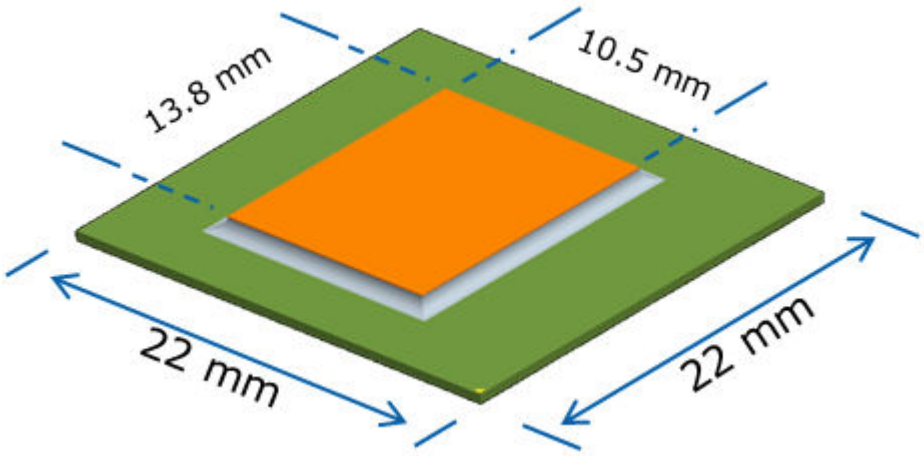

Figure 15 - Package Test Vehicle Model and Dimensional Overview

3.2.2 – Shock Test Board (STB) PCB Attributes:

A shock test board, or STB, is a PCB uniquely designed to test a specific component, or component type, in a dynamic drop use condition. Typically this type of test board is uniquely designed such that bend mode, flexure radius, chassis retention, and other variables representing a production design can be modulated, providing representative results to inform product designs. The STB specifically used within this evaluation has the following physical characteristics, from Intel Corporation (2008), all of which have a significant effect on the results and recommendations discussed.

Table 6 – STB PCB Attributes

STB Attribute	Value (Nominal)
X,Y Dimensions (PCB)	304.8 mm X 304.8 mm
PCB Thickness	1.016 mm
PCB Layer Count	10 Layer
PCB Surface Finish	OSP (Organic Solder Preservative)
Laminate Type	FR4, Mid-T_g

STB Attribute	Value (Nominal)
Integrated Strain Gage	Yes
PCB Pad Definition	SMD, 0.390 mm SRO MD, 0.390 mm
Via Definition	VOP (Via Off Pad)

Images of the STB used can be found below in Figure 16. The image on the left is an unassembled image of the entire 12” X 12” PCB. Note the drilled and copper plated holes used for mounting masses and modulating bend radius originating at the package center. Also, daisy chain breakout headers can be seen on the extreme east and west edges of the PCB. These points are where resistance is measured to indicate electrical performance throughout a specific test event. The image on the right is a close-up of reference designator U1, or the land of the package being tested. Noteworthy observations include detailed fault isolation test points on all sides of the package; prewired strain gage routing can be seen near all package corners, and silkscreen indicating solder joint location for ease of fault isolation and destructive failure analysis.

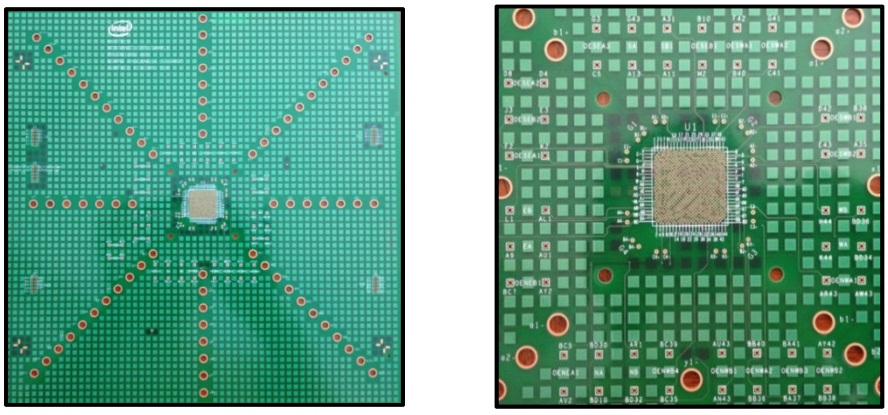

Figure 16 - Shock Test Board (STB)

4. Results and Discussion

4.1 – Summary of Results:

The following table provides a concise summary of results indicating whether the requirement was satisfied or not. Details can be reviewed in sections denoted in column 3.

Table 7 - Summary of Results

Requirement #	Pass / Fail	Reference (Section / Page)
1	Pass	4.2 / 22
2	Pass	4.3 / 23
3	Pass	4.4 / 25
4	Pass	4.5 / 28
5	Pass	4.6 / 28
6	Pass	4.7 / 29
7	Pass	4.8 / 30

4.2 – Preform Assembled by Pick and Place Equipment (Requirement #1):

Preformed SPEA, as illustrated on the corners of a component in Figure 17, was successfully placed onto the motherboard after the BGA component using standard nozzles on the Universal Genesis GSM1. All boards processed for further dynamic evaluation underwent preform placement via SMT.

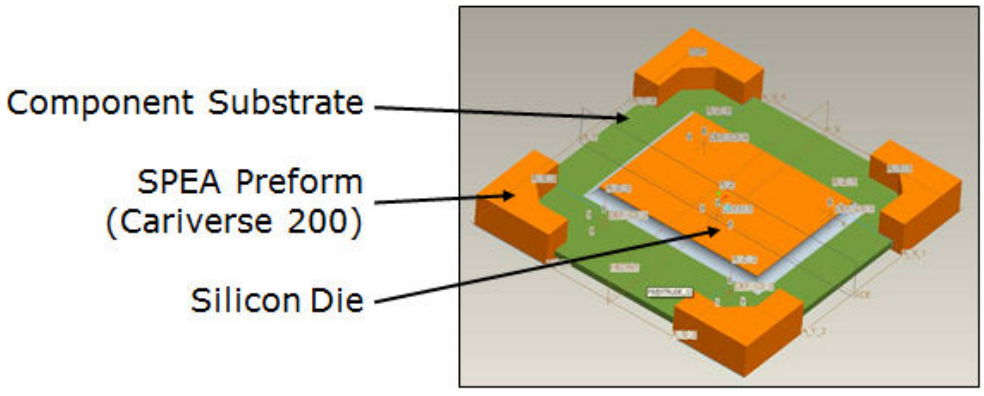

Figure 17 - SPEA Preform Illustration, Pre SMT

There was one occurrence of a preform being rejected by the component recognition camera. Upon further analysis, it was found that there was excess material on a single edge making it difficult for the system to verify component edge. Given that preforms were manufactured by hand, this issue is not unexpected or concerning. However, if ever in volume production, it is recommended to include a contrasting fidicual on the preform corner to help ensure high placement yields and accurate alignment.

4.3 – Reflow Process Parameters within Acceptable Range (Requirement #2):

A reflow profile was generated within recommended limits for Senju M705-GRN360-K2-Vi lead free solder paste (Senju, 2013); reference Appendix A for profile reference design. Table 7 outlines critical processing parameters, respective specifications, and as-measured results from sample materials. Again note that unique settings were not established specifically for SPEA, rather, requirements were met as inputs and post SMT assembly success indicators measured as outputs, indicating the effect of SPEA on assembly quality targets.

Table 8 - Reflow Processing Parameters

Parameter	Specification (Appendix A)	Measured
Rising (Heating) Rate	2.5-3.0 °C/second	2.2 °C/second
Soak	60-120 seconds (Senju M705-GRN360-K2-Vi)	102 seconds
Time Above Liquidus	40-120 seconds	68 seconds
Peak Temperature	240-250 °C	248 °C
Falling (Cooling) Rate	1.0-4.0 °C/second	1.2 °C/second

Although the oven is enclosed and it is not possible to witness the reflow cycle, it was observed that the shape of the preform, post SMT, was collapsed and relatively uniform, reference Figure 18. Under this evaluation, solid and collapsed preform shape was not specifically optimized, however, additional studies testing the effects of preform volume and geometry, would yield an ideal definition for maximum reliability.

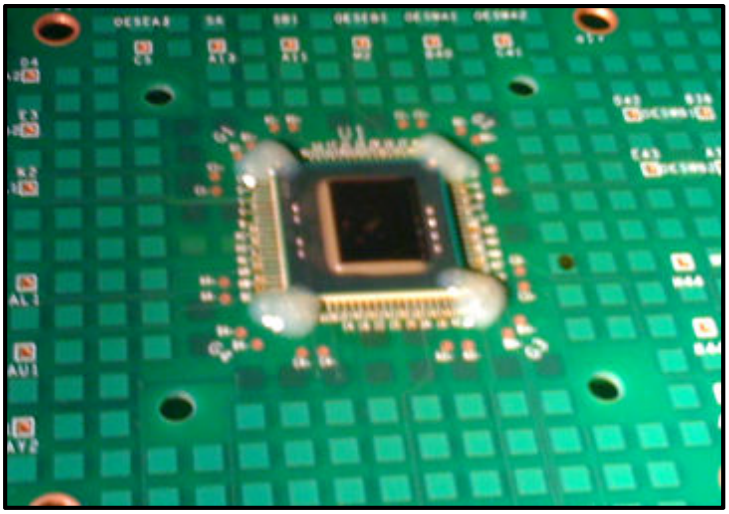

Figure 18 - Post SMT SPEA Formation

Observations indicate that the collapsed SPEA likely would exceed X-Y spatial keepout area's on a fully-populated motherboard. Alternatives to avoid this situation are to reduce SPEA volume or to increase the amount of adhesive material overhanging the package, essentially shifting the preform further towards the center of the package. It was also observed that the Z height of the post assembled SPEA did not exceed the height of the die. Consideration should be given to this when optimizing preform shape as BGA's typically have passive thermal solutions assembled at the system level.

4.4 – Post Assembly, Manufacturing Quality Indicators Achieved (Requirement #3):

The following indicators and related data are commonly collected post SMT as time-zero assessments of interconnect lifetime reliability. Industry standards bodies, like the

Industry Association for Printed Circuit Boards (IPC) and the Joint Electron Device Engineering Council (JEDEC), specify standards for the following attributes and are reflected in Table 2, requirement #3 (IPC-A-610D, 2005).

4.4.1 – Solder Bridging:

By definition solder bridging is the unintended joining of solder joints creating an electrical connection during electronics assembly. Per IPC's Acceptability of Electronic Assembly Standard, IPC-A-610-X (where X is the revision number); zero solder bridges are allowable in conductors not intended to be joined by design.

Of the 24 samples built within the experiment, there was no occurrence of solder bridging as tested both electrically (continuity) and via X-Ray. Figure 19 is an X-Ray image of an SPEA sample demonstrating expected and passing joint formation. Note that top side capacitors are placed on the component substrate and can be seen in the image. These are not to be mistaken with a solder bridge.

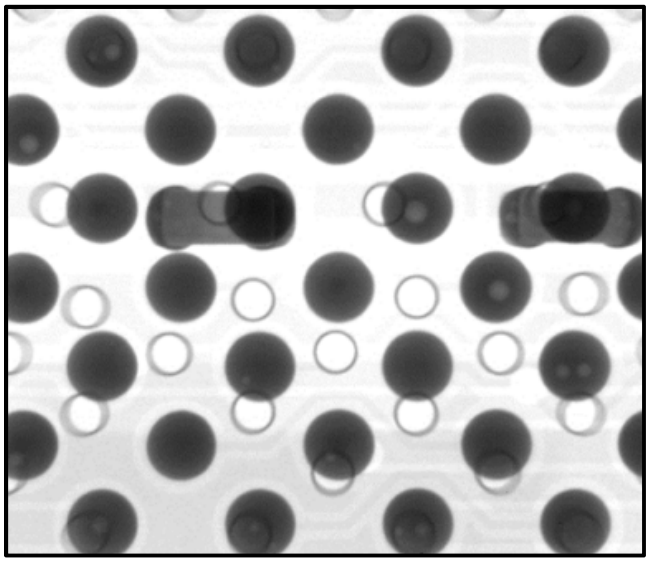

Figure 19 - X-Ray Image of BGA Solder Balls

4.4.2 – Solder Joint Voiding:

Also per the IPC-A-610-X specification, no more than 25% of the solder sphere's volume can be comprised of trapped moisture or oxygen, otherwise known as a void. Solder joint voiding is common and difficult to eliminate completely, however it has been found that reliability performance is sacrificed with voids in excess of 25%, hence the IPC standard. Voiding is primarily caused by moisture being trapped in the solder composition; typically moisture is outgassed and the solder fully coalesces, however, at times not all moisture is released. Baking moisture sensitive components prior to assembly and optimizing the reflow profile itself are both very important in limiting the amount of post assembly voiding.

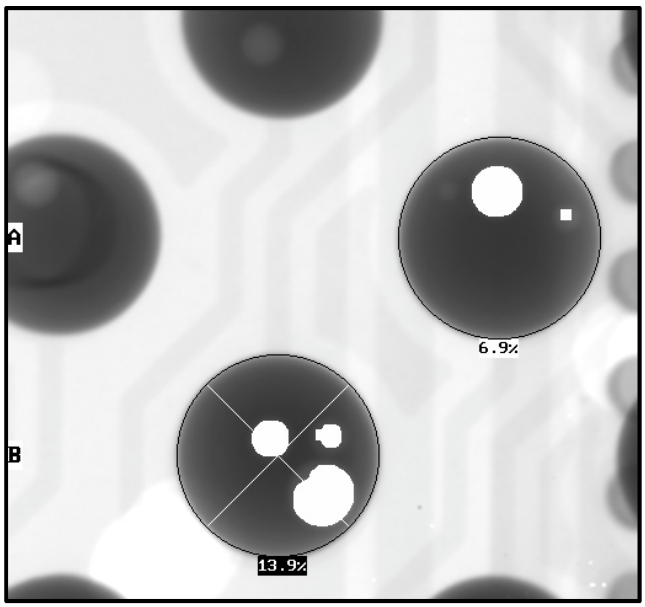

Figure 20 - Agilent 5DX X-Ray Image with Void Measurements

Voids are typically measured with multi-dimensional X-Ray machines and sophisticated software algorithms. During this experiment the Agilent Medalist 5DX machine was used to calculate void percentage. The equipment's algorithms measure

void area in two dimensions and extrapolate the measurements into the third dimension. The void area is then computed as a percentage of the solder ball diameter and presented on the screen. A statistically significant percentage of joints were measured from joints visually inspected to be of high voiding. No solder joints exceeded IPC's specification of 25% voiding. A representative example of solder joint voiding and the 5DX output can be seen in Figure 20.

4.4.3 – Package Standoff Height:

Failure Mode and Effects Analysis (FMEA), described by Wikipedia as a systemic technique used for predictive analysis of system reliability (Failure mode and effects analysis, 2013), suggested package standoff height to be a primary area of risk given the opportunity for SPEA to flow under the package prior to solder solidification. The identified risk hypothesized that the SPEA material would limit the package settling in the –Z direction, caused naturally through the coalescence of solder onto the land pads.

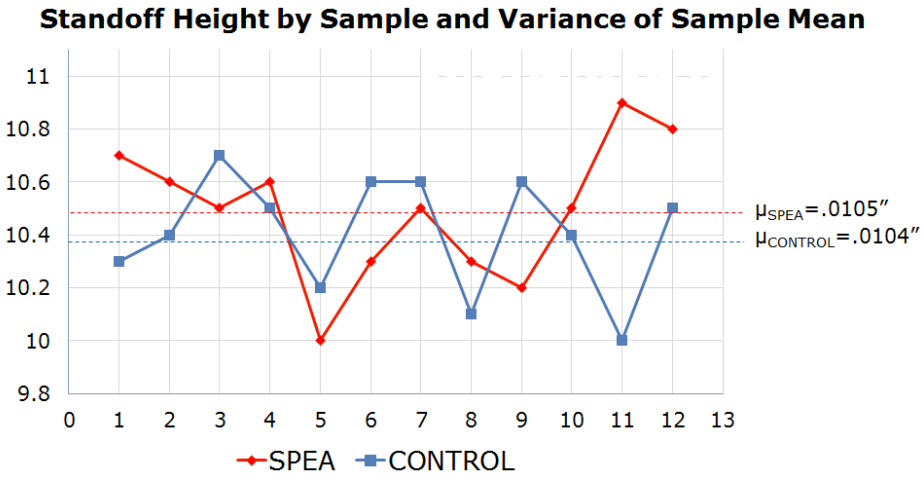

Figure 21 - Package Standoff Height Comparison: SPEA vs. CONTROL

With regards to BGA SMT manufacturing, the post reflow solder joint profile is critical to the assembly's life-reliability performance. Joints that are elongated and joints that

are overly compressed exhibit a reduction in reliability performance. Therefore, detailed analysis was performed specifically to ensure that SPEA sample standoff height was not statistically different to the control samples using no adhesive.

Data collected and represented in Figure 21 shows that although SPEA assembled packages show a statistically higher average standoff height, the increase is not significant: 10.38 mil average for the control leg and 10.49 for the SPEA leg, satisfying the requirement.

Note that package standoff height data is collected via cross sectional analysis as described in section 2.2.4. Representative samples of cross sectional images can be found below, in Figure 22.

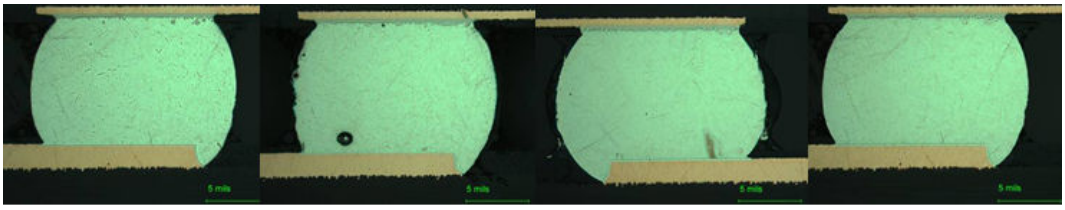

Figure 22 - Solder Joints in Cross Sectional View

4.4.4 – Solder Joint Formation:

It is common for an experienced engineer to perform a qualitative assessment of joint formation, including void location, grain structure, intermetallic layer thickness, and other indicators to the quality of the solder joint. Figure 22 represents randomized selection of cross sectional views taken from this analysis and there are no unexpected or notable observations drawn from the images. Solder joint formation is as expected.

4.5 – Rework Process Parameters within Acceptable Range (Requirement #4):

Similar to SMT reflow, there are critical thermal parameters which have been proven to yield optimized solder joints in rework. Those parameters and results are listed below in Table 6. Further details on rework profile targets can be found in Appendix B. All measured results fall within expected process windows and are considered passing.

Table 9 - Rework Processing Parameters

Parameter	Specification (Appendix B)	Measured
Rising (Heating) Rate	0.5-2.5 °C/second	1.3 °C/second
Soak	≤ 120 seconds (Senju M705-GRN360-K2-Vi)	102 seconds
Time Above Liquidus	60-120 seconds	83 seconds
Peak Temperature	230-250 °C	242 °C
Falling (Cooling) Rate	0.5-2.0 °C/second	1.4 °C/second

4.6 – SPEA Fully Removed Post Rework (Requirement #5):

A firm industry requirement for the use of any SMT adhesive is that it must be fully reworkable, meaning that the original package placed during SMT can be removed and the package site clean for assembly, or rework, of another component.

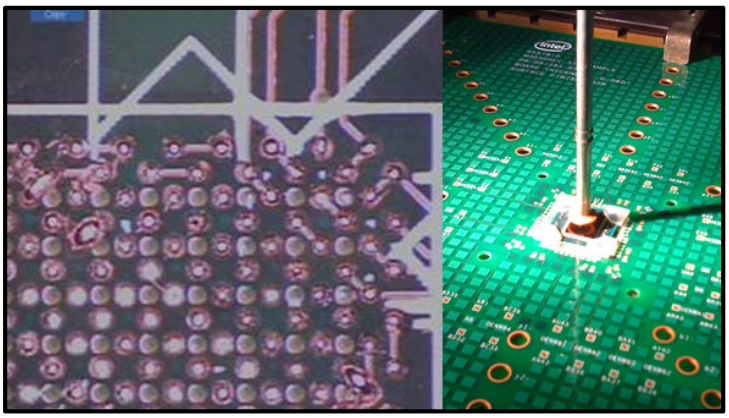

Figure 23 - SPEA Rework, Removal and Package Replacement

Two samples were tested to ensure that the material could be removed from the PCB, and both tests passed. SPEA was removed using common materials including Isopropyl Alcohol (IPA) and heat. Images of the reworked site and reassembly of another SPEA package can be found in Figure 23.

4.7 – $\Omega_{CONTROL} = \Omega_{SPEA}$ at Capability Cliff (Requirement #6):

Leveraging additional testing performed outside of the scope of this assessment, a maximum allowable strain value of 3650με was derived for the component and PCB being tested (Intel Corporation, 2007). Published strain values always include a margin of safety, and given this became the initial input value tested. Using an assembled board to setup the shock table, the strain value was achieved based on a given input of approximately 175G. At this point in the testing, the resistance measured at the outermost daisy chains was equivalent between SPEA and non SPEA samples, approximately 18Ω for all samples, hence successfully meeting requirement #6.

4.8 – Increased Dynamic Reliability, ε_{MAX} (Requirement #7):

Building upon section 4.7, input G levels were incrementally increased by approximately 25G from the 175G, 3650με baseline, and strain measured during each stepping. Results of this analysis have been summarized in Figures 24 and 25. Detailed data logs', including input G stepping's and computed strain, can be found in Appendix E - Dynamic Shock, Analyzed Data Logs. Results from the control group, samples C1, C2, and C3 demonstrate an average maximum allowable strain of 4148με. Note that discrete values being aggregated are from the test prior to the failed test, the maximum achievable strain value discernible through consistent electrical continuity.

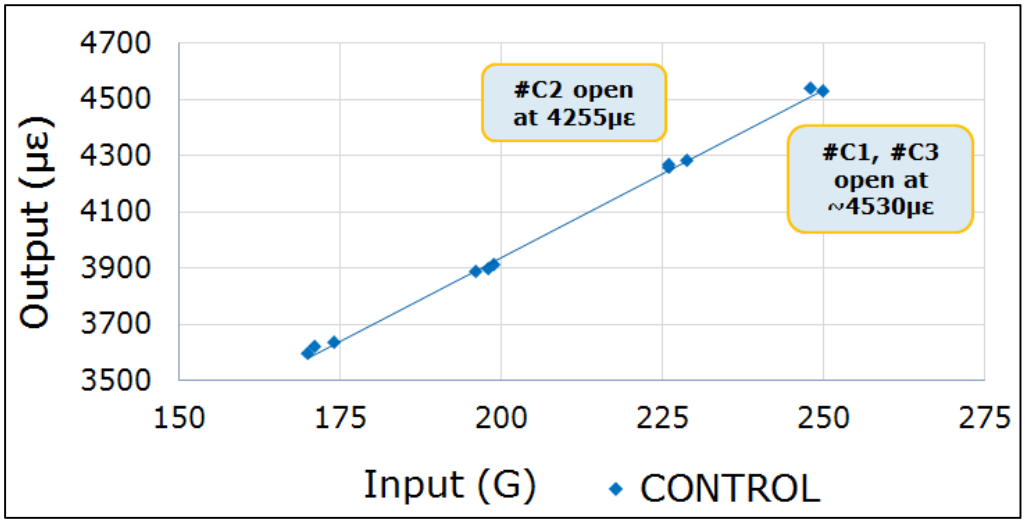

Figure 24 – Control Leg, Strain Results Summary

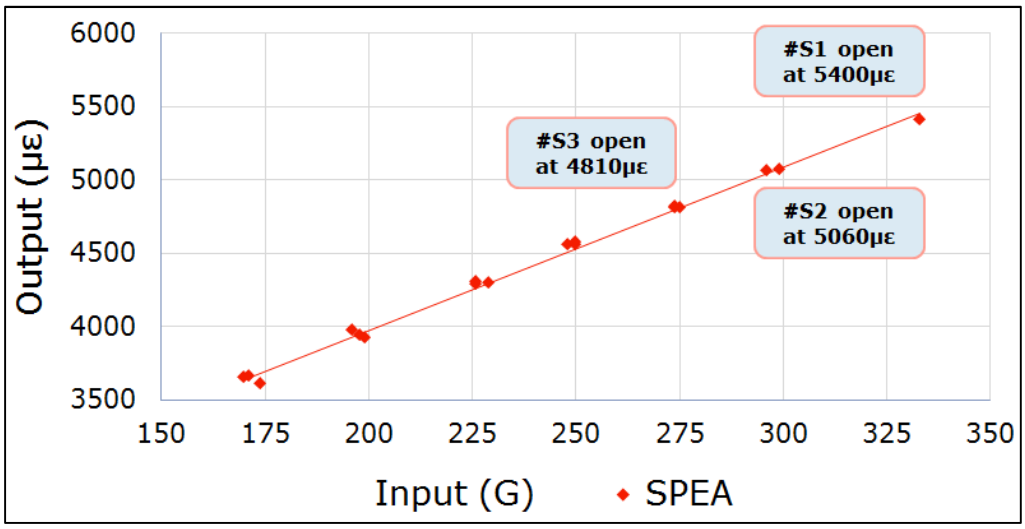

Figure 25 – SPEA Leg, Strain Results Summary

Results from the SPEA group, samples S1, S2, and S3, demonstrate a maximum allowable strain of 4801με, an average increase of 15.8% allowable strain over the control group. Although specific margin increase values were not detailed in the requirement, the performance increase achieved is significant. More importantly, all SPEA samples have an increased allowable strain limit over all control samples, demonstrating consistency in the application and dynamic shock performance margin gain.

5. Conclusions and Recommendations

All areas for which SPEA was evaluated successfully met predefined requirements for both manufacturability and dynamic reliability. With regards to manufacturability, the material, its formation, and application process was seamlessly integrated into a typical electronic motherboard manufacturing line without the need for unique equipment, alterations, or additional manual processes. With regards to dynamic reliability, SPEA provided consistent dynamic margin increase across samples. When compared to the non-adhesive control group SPEA demonstrated a 15.8% increase in allowable strain. Although, while technical requirements under this evaluation were met, there are many other factors and considerations that must be optimized prior to SPEA being ready for high volume applications. As discussed previously, follow-on areas of study should include the following:

1. Pre-Defined Shape: As discussed in section 4.3, additional studies evaluating the pre-assembled shape of SPEA preforms would yield an optimized size and center of gravity. As observed during this study, material flow beyond a typical keepout zone for a package of this type and application is of concern, and might be remedied through an alternate formation. Further, evaluating the dynamic effect of lengthening the preform along the edge of each package corner could prove fruitful. Future analysis should be based on typical joint failure locations with a known preform shape to understand the potential effect of increased length in SPEA.

2. Volumetric Effects: Expanding on the necessity for an optimized shape, effects of material volume on dynamic reliability is a critical area of focus. It is conceivable

to hypothesize that a reduction in volume would increase package to board conformance during a dynamic event, effectively reducing rigidity. One could argue, however, that less material dilutes overall surface area bonding resulting in a less capable assembly. Both projections seem feasible and a detailed evaluation of both shape and volume could yield a much more optimized solution.

3. Cost Modeling: As always, real world costs and cost targets need to be evaluated during any technology feasibility assessment. These considerations often become the basis for what and how technical solutions are implemented. A detailed cost model evaluating all aspects of the supply chain including raw materials, pre-assembly formation, packaging and distribution should be conducted. At the time of this study, preliminary analysis suggested that each preform would nominally cost $0.064 at a volume of approximately 600,000 units. Further justifying implementation, a thorough ROI analysis should be conducted specifically focusing on a decrease in RMA and an increase in sales volumes given expanded package capabilities.

SPEA is a proven viable alternative to current industry electronics adhesive with the demonstrated ability to reduce manufacturing throughput time while increasing application consistency and in turn dynamic reliability.

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Glossary of Terms

ATV **Assembly Test Vehicle** - A physically representative, yet nonfunctional, electronic package used to test and qualify manufacturing and assembly techniques.

BGA **Ball Grid Array** - An electronic package type where solder balls are assembled onto a substrate interface between the silicon and printed circuit board.

CM **Contract Manufacturer** - A manufacturer that contracts with a firm for components or products.

CPU **Central Processing Unit** - Is the hardware within a computer that carries out the instructions of a computer program by performing the basic arithmetical, logical, and input / output operations of the system.

DCTV **Daisy Chain Test Vehicle** - A physically representative electronic package that, when mated to a corresponding printed circuit board is designed to create an electrically continuous chain.

DfR **Design for Reliability** - A process by which specific considerations are made during the design of a product in order to meet end use environmental requirements of the product.

FMEA **Failure Modes Effects and Analysis** - A methodology of systemic techniques used for predicting reliability failures and associated analysis.

G **Gravity** - 9.81 m/s^2, or 32.2 $ft./s^2$

HVM **High Volume Manufacturing** - A manufacturing environment producing large quantities of goods in short periods of time, often employing the use of automated machines and equipment.

IEEE **Institute of Electrical and Electronics Engineers** - A professional association headquartered in New York City that is dedicated to advancing technological innovation and excellence in electronics.

IO **Input / Output** - A unique electrical connection carrying either an inbound or outbound signal from a processing device.

IPC **Industry Association for Printed Circuit Boards** - A member-driven organization focused on all facets of the electronic interconnect industry including design, printed circuit board manufacturing and electronics assembly.

JEDEC **Joint Electron Device Engineering Council** - An industry driven committee focused on developing open standards for the microelectronics industry.

LF **Lead Free -** A solder composition which does not contain lead (Pb).

MD **Metal Defined** - Referring to a land, or connection point on a printed circuit board, that does not have soldermask encroaching on the edges of the etched copper.

ODM **Original Design Manufacturer** - A company which designs and manufactures a product which is specified and eventually branded by another firm for sale.

OEM **Original Equipment Manufacturer** - A company who manufactures product or components that are purchased by another company and retailed under the purchasing company's brand name.

PCB **Printed Circuit Board** - A three dimensional array of electrical interconnects built between layers of dielectric and used to both electrically a mechanically connect electronic components.

PDA **Personal Digital Assistant** - A mobile device that functions as a personal information manager.

SLI **Second Level Interconnect** - The electrical connection between an electronic package and the printed circuit board on which it is mounted. Note that the first level interconnect refers to the electrical connection between the silicon die and the substrate.

SMD **Solder Mask Defined** - Referring to a land, or connection point on a printed circuit board, that has soldermask encroaching over the edges of the etched copper.

SMT **Surface Mount Technology** - Automation equipment in the electronics manufacturing industry used to assemble raw electrical components onto a printed circuit board. Typically consists of a paste print machine, pick and place machine, thermal reflow oven, and an automated optical inspection machine.

SPEA **Solid State Preformed Electronics Adhesive** - An electronics adhesive, specifically Cariverse 200, that is molded into solid preforms which are assembled onto electronic packages by pick and place equipment prior to thermal reflow.

SRO **Solder Resist Opening** - A circular opening in soldermask, a coating used to impede electrical flow, allowing electrical connectivity. Typically associated with a solder mask defined land.

STB **Shock Test Board** - A printed circuit board specifically designed to evaluate multiple types of dynamic reliability testing.

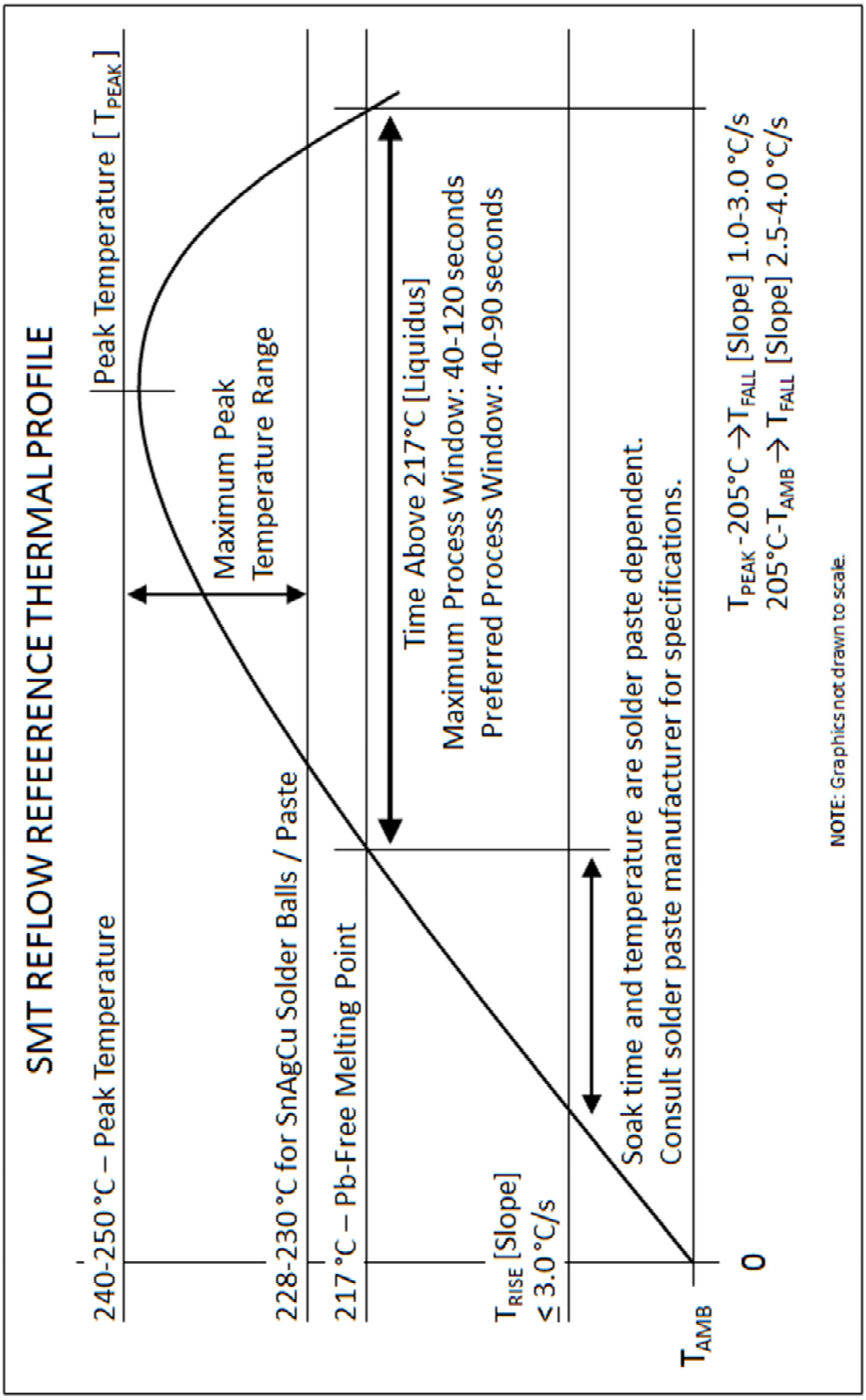
TAL **Time Above Liquidus** - The amount of time during a lead free thermal reflow that the solder joints are above 217 degrees Celsius.

TMA **Thermomechanical Analysis** - A technique used in thermal analysis which studies the properties of materials as they change with temperature.

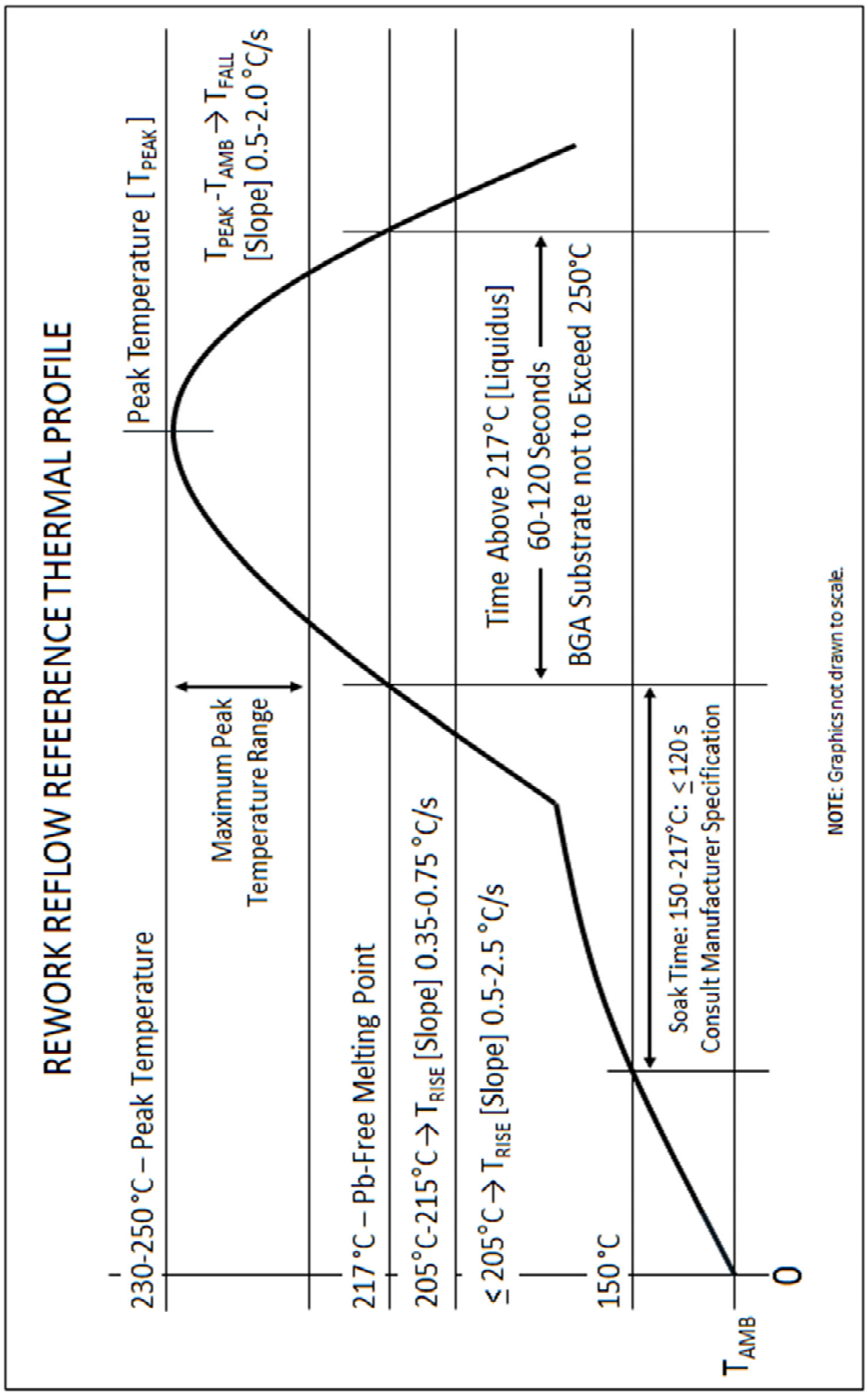
TTV **Thermal Test Vehicle** - A physically representative, yet nonfunctional, electronic package such that when voltage is applied heats to represent operating thermal conditions of a functional system.

VOP **Via Off Pad** - Referring to a via, an electrical connection made between printed circuit board layers by plating drilled holes, that is not in the land (pad) where the connection between the electrical component and the printed circuit board is made.

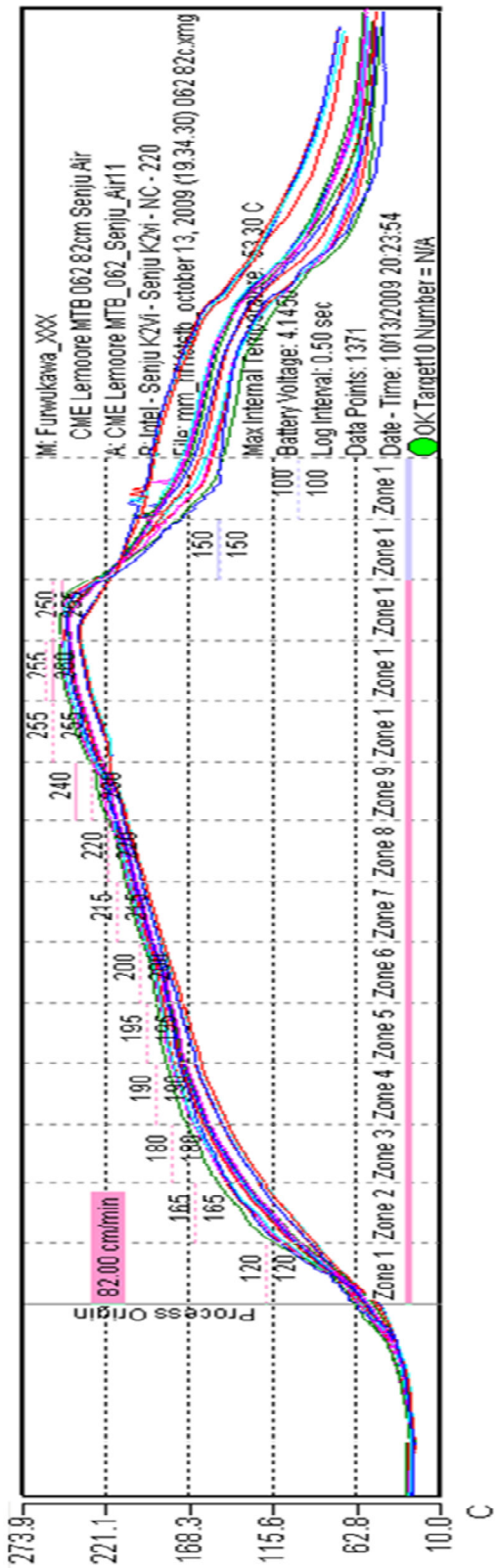
Appendix A – Lead Free, SMT Reflow Reference Thermal Profile



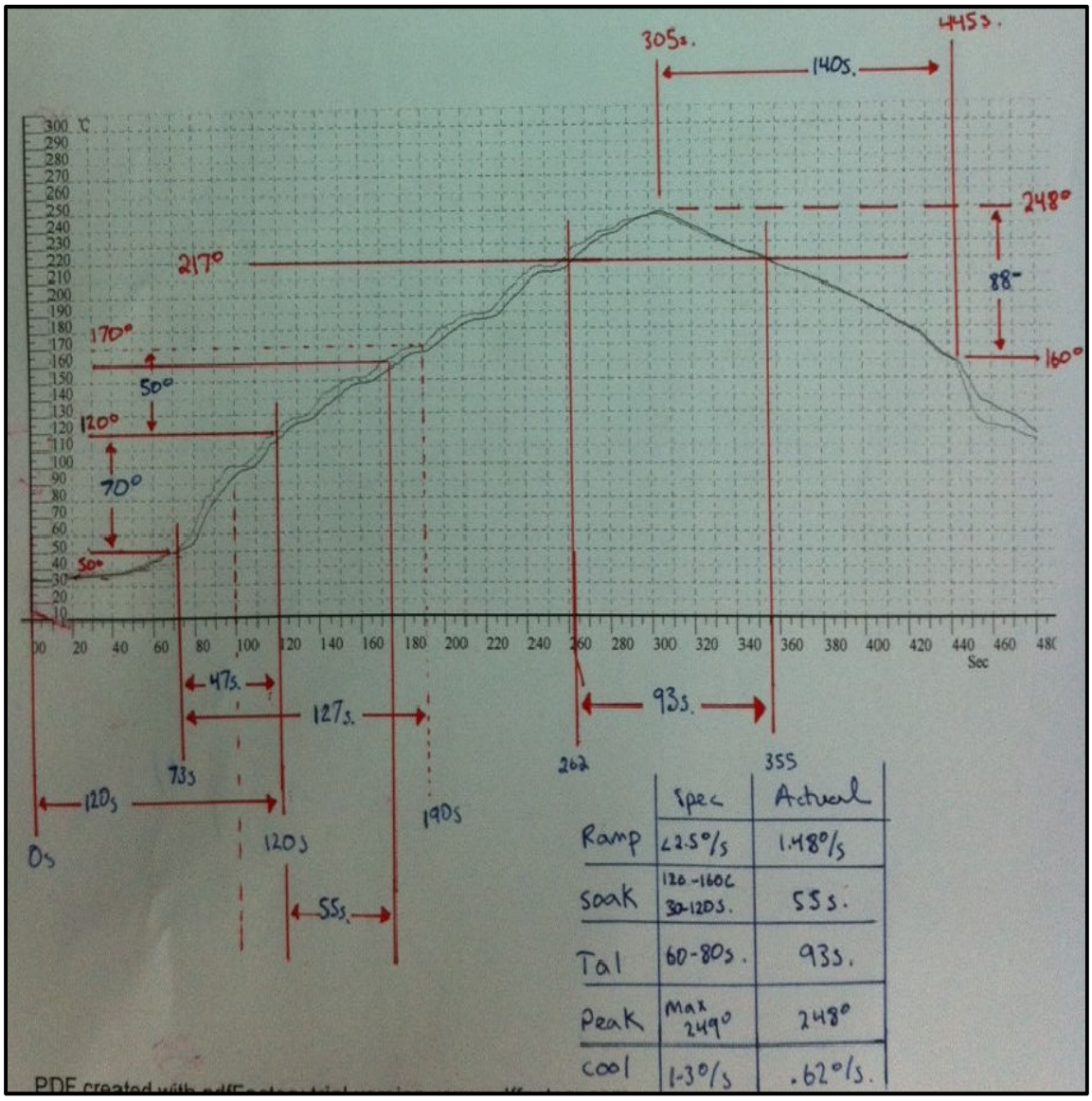
Appendix B – Lead Free, Rework Reflow Reference Thermal Profile



Appendix C – Lead Free Thermal Profile Thermocouple Trace



Appendix D – Common Thermal Profile Assessment Technique (By Hand)



RAW DATA

TEST #	SAMPLE #	ACCELEROMETER (Input G)	SPEA LEG		CONTROL LEG	
			COMPUTED STRAIN εd (με)	Pass / Fail	COMPUTED STRAIN εd (με)	Pass / Fail
1	C1, S1	170	3640	P	3590	P
2	C1, S1	196	3970	P	3880	P
3	C1, S1	226	4278	P	4260	P
4	C1, S1	250	4550	P	4525	F
5	S1	274	4805	P		
6	S1	296	5055	P		
7	S1	333	5400	F		
8	C2, S2	171	3655	P	3617	P
9	C2, S2	199	3910	P	3905	P
10	C2, S2	226	4295	P	4255	F
11	S2	250	4565	P		
12	S2	275	4800	P		
13	S2	299	5060	F		
14	C3, S3	174	3600	P	3630	P
15	C3, S3	198	3933	P	3893	P
16	C3, S3	229	4290	P	4278	P
17	C3, S3	248	4548	P	4535	F
18	S3	274	4810	F		

PASSING STRAIN LEVELS

CONTROL LEG	
SAMPLE #	PASSED STRAIN (με)
C1	4260
C2	3905
C3	4278
AVERAGE	4147.67

SPEA LEG	
SAMPLE #	PASSED STRAIN (με)
S1	5055
S2	4800
S3	4548
AVERAGE	4801

STRAIN MARGIN

MIN	0.0631136	6.31%
MAX	0.2944942	29.45%
AVERAGE	0.1575183	15.75%